ESP-12F WIFI Module Datasheet

Version 1.1

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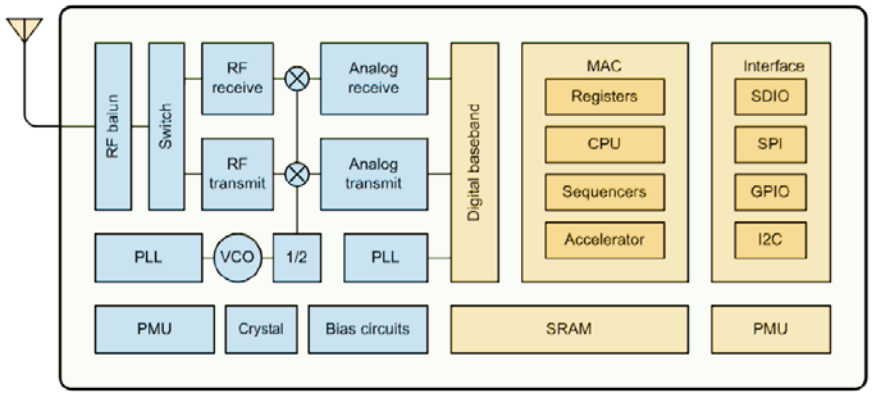
1 Overview

1.1 Introduction

ESP-12F WIFI modules is provided by Huash-Fly that integrates ESP8266EX. The module has been adjusted to get the best RF performance.

ESP8266EX is high integration wireless SOCs, designed for space and power constrained mobile platform designers. It provides unsurpassed ability to embed Wi-Fi capabilities within other systems, or to function as a standalone application, with the lowest cost, and minimal space requirement.

Figure 1 ESP8266EX block Diagram



ESP8266EX offers a complete and self-contained Wi-Fi networking solution. Is can be used to host the application or to offload Wi-Fi networking functions from another application processor.

When ESP8266EX hosts the application, it boots up directly from an external flash. It has been integrated cache to improve the performance of the system in such applications.

Alternately, serving as a Wi-Fi adapter, wireless internet access can be added to any microcontroller-based design with simple connectivity through UART interface or the CPU AHB bridge interface.

ESP8266EX is among the most integrated WIFI chip in the industry. It is integrated the antenna switches, RF balun, power amplifier, low noise receive amplifier, filters, power management modules,. It requires minimal external circuitry, and the entire solution, including front-end module, is designed to occupy minimal PCB area.

ESP8266EX is also integrated an enhanced version of Tensilica's L106 Diamond series 32-bit processor, with on-chip SRAM, besides the Wi-Fi functionalities. ESP8266EX is often integrated with external sensors and other application specific devices through its GPIOs. Codes for such applications are provided in examples in SDK.

Sophisticated system-level features include fast sleep/wake context switching for energy-efficient VoIP, adaptive radio biasing for lov-power operation, advance signal processing, and spur cancellation and radio co-existence features for common cellular, Bluetooth, DDR, LVDS, LCD interference mitigation.

1.2 Features

◆ **SOC Features**

- Build-in Tensilica L106 32-bit industry-leading ultra low powe MCU, with 80MHz or 160MHz clock
- Integrated TCP/IP protocol stack
- Integrated 1 channel 10-bit ADC
- Supported HSPI, UART, I2C, I2S, IR remote Control, PWM, GPIO
- Power down leakage current < 10 uA
- Wake up and transmit packets in < 2ms
- Standby power consumption of < 1.0mW (DTIM3)

◆ **Wi-Fi Features**

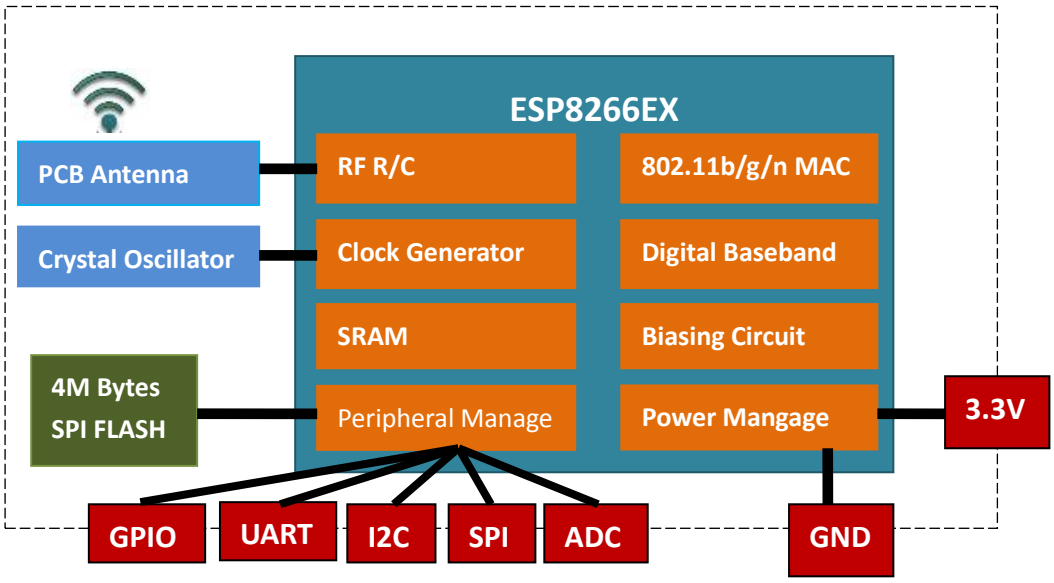
- 802.11 b/g/n protocol
- Supported CCMP (CBC-MAC, Counter Mode), TKIP (MIC, RC4), WAPI (SMS4), WEP (RC4), CRC hardware Acceleration
- WPA/PA2 PSK/WPS
- Integrated TR switch, balun, LNA, power amplifier and matching network
- Integrated PLL, regulators, and power management units

◆ **Module Features**

- PCB-on-board antenna
- SMT and DIP-2.54mil package interface

1.3 Module Block Diagram

Figure 2 Module Block Diagram



1.4 Parameters

Table 1 Module Parameters

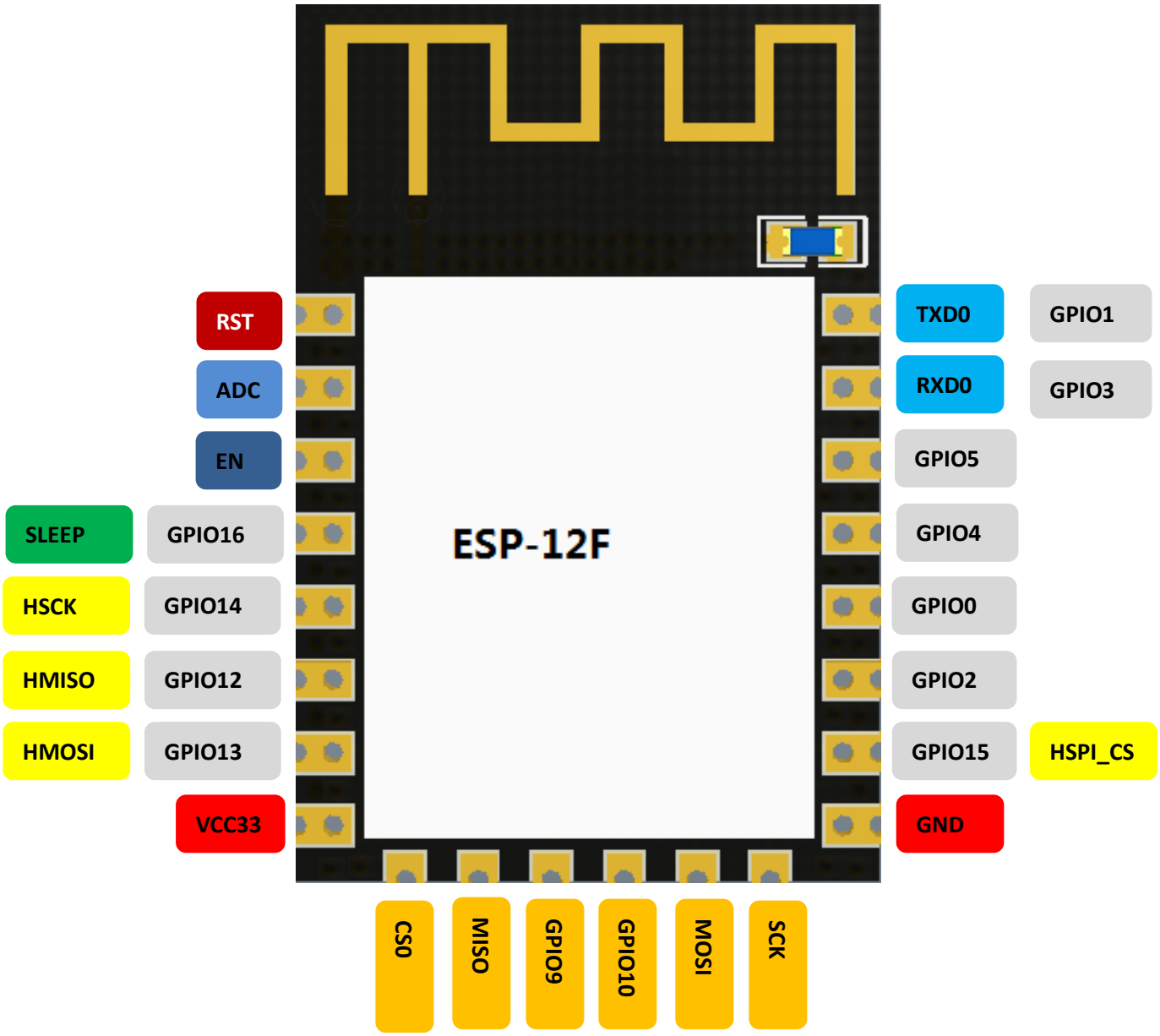
Types	Items	Parameters
Wi-Fi	Frequency Range	2.4G~2.5G(2400MHz~2483.5MHz)
	Transmitting Power	802.11b: +20 dBm
		802.11g: +17 dBm
		802.11n: +14 dBm
	Receiving Sensitivity	802.11b: -91 dBm (11Mbps)
		802.11g: -75 dBm (54Mbps)
		802.11n: -72 dBm (MCS7)
Hardware	CPU	Tensilica L106 32-bit MCU
	Interface	UART/SDIO/SPI/HSPI/I2C/I2S/IR/GPIO/ADC/PWM
	Work Voltage	2.5V~3.6V
	Work Average Current	80mA
	Work Temperature	-40~85℃
	Storage Temperature	-40~125℃
	Package Size	16mm x 24mm x 3mm
Software	Wi-Fi Mode	Station/SoftAP/SoftAP+Station
	Security	WPA/WPA2
	Encryption	WEP/TKIP/AES
	Firmware Upgrade	UART Download / OTA (via network) / download and write firmware via host
	Software Development	Supports Cloud Server Development / SDK for custom firmware development
	Network Protocols	IPv4, TCP/UDP/HTTP/FTP
	User Configuration	AT Instruction Set, Cloud Server, Android/iOS App

2. Interface Definition and Description

2.1 Module Interface definition

Following show the definition of peripheral interface, include the main function and the second function.

Figure 3 Module interface definition



2.2 Working Mode Selection

GPIO15, GPIO0 and GPIO0 can select different working mode. Following table show the working mode of module.

Table 2 Working mode selection

MODE	GPIO15	GPIO0	GPIO2
UART download mode	Low	Low	High
Flash Boot mode	Low	High	High

2.3 PIN Interface Function Description

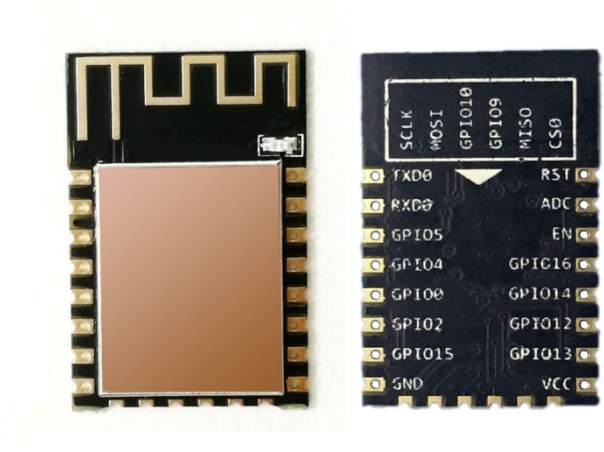
Table 3 Pin interface function description

No.	PIN Name	Type	Function Description
1	RST	I	External reset signal (Low level effective)
2	ADC	I	10-bit ADC , input voltage range: 0~1V; value range: 0~1024
3	EN	I	Chip enabled. IC could work while high level. IC could be shut off while low level.
4	GPIO16	I/O	Wake up from deep sleep mode
5	GPIO14	I/O	GPIO14; HSPI_CLK
6	GPIO12	I/O	GPIO12; HSPI_MISO
7	GPIO13	I/O	GPIO13; HSPI_MOSI; UART0_CTS
8	VCC33	P	3.3V Mode power
9	CS0	I/O	GPIO11; SD_CMD; SPI_CS0
10	MISO	I/O	GPIO7; SD_D0; SPI_MISO
11	GPIO9	I/O	GPIO9; SD_D2; HSPIHD
12	GPIO10	I/O	GPIO10; SD_D3; SPIWP; HSPIWP
13	MOSI	I/O	GPIO8; SD_D1; SPI_MOSI
14	SCLK	I/O	GPIO6; SD_CLK; SPI_CLK
15	GND	P	Power Ground
16	GPIO15	I/O	GPIO15; MTD0; HSPI_CS;
17	GPIO2	I/O	GPIO2, UART1_TXD
18	GPIO0	I/O	GPIO0; SPI_CS2
19	GPIO4	I/O	GPIO4
20	GPIO5	I/O	GPIO5
21	RXD0	I/O	GPIO3 and UART RXD.
22	TXD0	I/O	GPIO1 and UART TXD.

3. Appearance and Dimension

3.1 Module Appearance

Figure 4 Module Appearance



3.2 Module Package and Dimision

The pin distribution of the module is illustrated in Figure 5. and Figure 6

Figure 5 Top view dimension

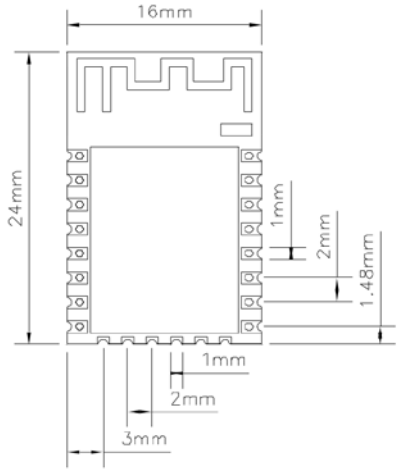


Figure 6 Side view dimension

The following data illustrates the size of the module.

Table 4 Module size table

Length	Width	Height	Bottom PAD Size	Gap between pin
16 mm	24 mm	3 mm	0.9mm x 1.9 mm	2 mm

4. Electrical Characteristics

Table 5 Electrical Characteristics

Item		Conditions	Min	Type	Max	Unit
Storage Temperature		-	-40	20	125	℃
Max SMT Temperature		IPC/JEDEC J-STD-020	-	-	260	℃
Work Voltage		-	2.5	3.3	3.6	V
I/O	V_{IL}/V_{IH}	-	$-0.3/0.75V_{IO}$	-	$0.25V_{IO}/3.6$	V
	V_{OL}/V_{OH}	-	$N/0.8V_{IO}$	-	$0.1V_{IO}/N$	V
	I_{MAX}	-	-	-	12	mA

5. Power Comsumption

Table 6 Power comsumption

Mode	Min	Type	Max	Unit
Tx 802.11b, CCK 11Mbps, POUT=+17 dBm	-	170	-	mA
Tx 802.11g, OFDM 54Mbps, POUT=+15 dBm	-	140	-	mA
Tx 802.11n, MCS7, POUT=+13dBm	-	120	-	mA
Rx 802.11b, 1024 Bytes Package, -80 dBm	-	50	-	mA
Rx 802.11g, 1024 Bytes Package, -70 dBm	-	56	-	mA
Rx 802.11n, 1024 Bytes Package, -65 dBm	-	56		mA
Modem-sleep①	-	15	-	mA
Light-sleep②	-	0.9	-	mA
Deep-sleep③	-	20	-	μA
Shut down	-	0.5	-	μA

6. Wifi RF Characteristics

The following are measured under room temperature conditions with 3.3V and 1.1V power supplies.

① Modem-sleep requires the CPU to be working, as in PWM or I2S applications. According to 802.11 standards (like U-APSD), it saves power to shut down the Wi-Fi Modem circuit while maintaining a Wi-Fi connection with no data transmission. E.g. in DTIM3, to maintain a sleep 300ms-wake 3ms cycle to receive AP's Beacon packages, the current is about 15mA.

② During Light-sleep, the CPU may be suspended in applications like Wi-Fi switch. Without data transmission, the WI-Fi Modem circuit can be turned off and CPU suspended to save power according to the 802.11 standard (U-APSD). E.g. in DTIM3, to maintain a sleep 300ms-wake 3 ms cycle to receive AP's Beacon packages, the current is about 0.9mA.

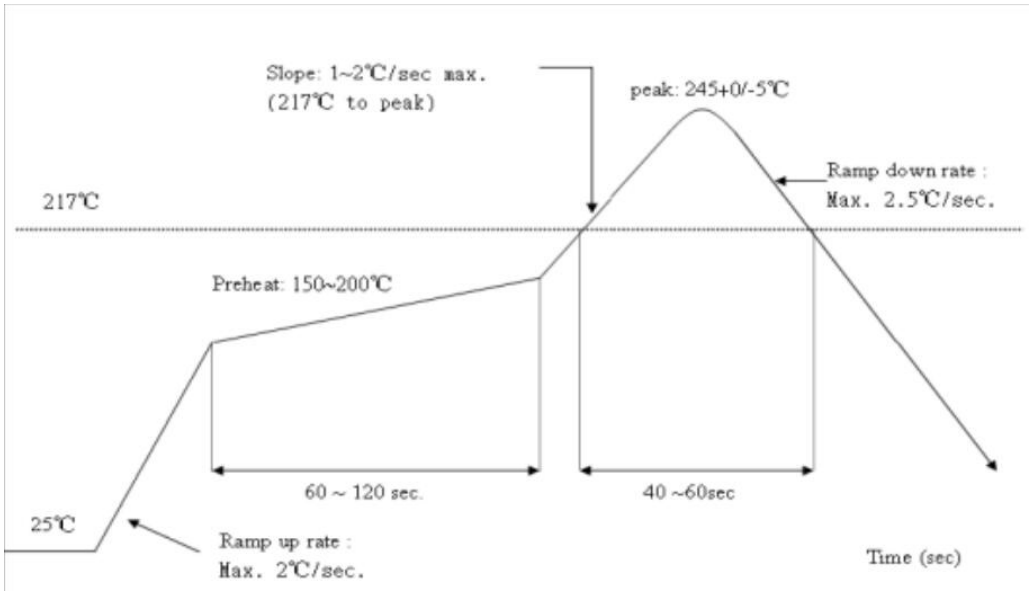
③ Deep-sleep does not require Wi-Fi connection to be maintained. For application with long time lags between data transmission, e.g. a temperature sensor that checks the temerature every 100s, sleep 200s and waking up to connect to the AP (taking about 0.3~1s), the overall average current is less than 1ms.

Table 7 Wi-Fi RF characteristics

Description	Min	Type	Max	Unit
Input Frequency	2412	-	2484	MHz
Input Impedance	-	50	-	Ω
Input Reflection	-	-	-10	db
Output Power of PA for 72.2Mbps	15.5	16.5	17.5	dBm
Output Power of PA for 11b mode	19.5	20.5	21.5	dBm
DSS, 1Mbps	-	-98	-	dBm
CCK, 11Mbps	-	-91	-	dBm
6Mbps (1/2 BPSK)	-	-93	-	dBm
54Mbps(3/4/64-QAM)	-	-75	-	dBm
H20, MCS7 (65Mbps, 72.2Mbps)	-	-72	-	dBm
Adjacent Channel Rejection				
OFDM, 6Mbps	-	37	-	dB
OFDM, 54Mbps	-	21	-	dB
HT20, MCS0	-	37	-	dB
HT20, MCS7	-	20	-	dB

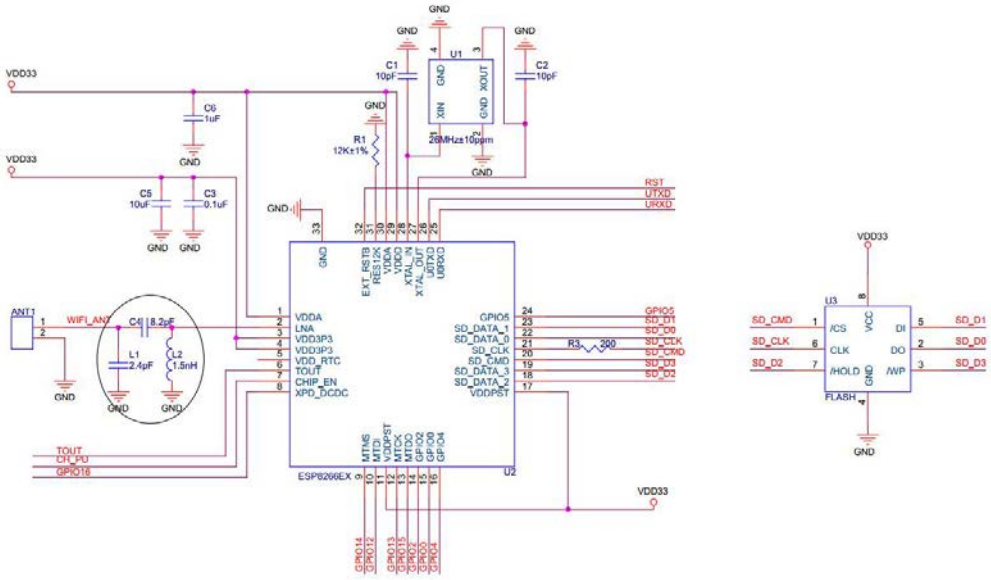
7. Recommended Reflow Temperature Diagram

Figure 7 Recommended reflow temperature diagram



8 Module schematics

Figure 8 Module schematics



9 Module Basic Application System

Figure 9 Module Basic Application System